SGS-THOMSON MICROELECTRONICS

STV2161

VIDEO SCANNING PSI PROCESSOR

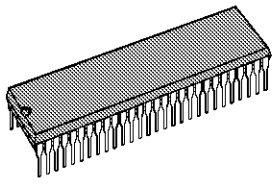
ADVANCE DATA

VIDEO PART

- RGB INPUT WITH FAST BLANKING SWITCH FOR SCART CONNECTOR
- RGB INPUT WITH FAST BLANKING FOR ON SCREEN DISPLAY / TELETEXT
- USER CONTROL FUNCTIONS : CONTRAST, BRIGHTNESS, SATURATION
- AVERAGE BEAM LIMITER FUNCTION WITH CONTRAST AND BRIGHTNESS REDUCTION
- PAL/SECAM OR NTSC MATRIX SWITCHABLE BY BUS
- AUTOMATIC CUTOFF LOOP WITH INTEGRATED DIGITAL MEMORY AND LEAKAGE CURRENT COMPENSATION
- CUTOFF REGISTER STATUS READABLE BY BUS
- FULL WHITE (DRIVE) ADJUSTMENT VIA BUS (NO CONTROL LOOP)
- BUS REPLY : FAST BLANKING SIGNAL RECOGNITION FOR POSITIVE AND NEGATIVE LEVEL / TUBE COLD INFORMATION
- OVERSIZE BLANKING FOR VERTICAL AND HORIZONTAL OVERSIZE
- APX (AUTO-PIX) : ADAPTIVE CONTRAST CONTROL
- COLOR MATCHING (IN CONNECTION WITH WHITE STRETCH ; SEE PSI PART)
- APL (AUTO-PEDESTAL) = ADAPTIVE BRIGHTNESS (IN CONNECTION WITH BLACK STRETCH ; SEE PSI PART)

SCANNING PART

- SYNC SEPARATOR WITH BLACK LEVEL CLAMP BASED ON CURRENT RATIO 1:8
- PHI1 LOOP WITH COMPLETELY INTEGRATED CALIBRATED RC OSCILLATOR (NO EXTERNAL CERAMIC) AND EXTERNAL LOOP FILTER
- PHI1 PHASE POSITION SELECTABLE BY BUS FOR COMB FILTER APPLICATION
- VCR AND TV MODE (SELECTION OF CURRENT) FOR PHI1 LOOP FILTER
- AUTOMATIC SYNC PRESENCE DETECTION AND AUTOMATIC PHI1 MUTE (FREE RUN ING) MODE (IMPROVED COMPARED TO STV2160)
- SYNCHRONISATION OUTPUT FOR VIDEO TEXT AND OSD DISPLAY
- PHI2 LOOP WITH INTERNAL LOOP FILTER
- PULSE OUTPUT FOR DRIVING HORIZONTAL OUTPUT STAGE
- HORIZONTAL DRIVE STANDBY VOLTAGE >V_{CC} POSSIBLE (12V MAX)
- VERTICAL COUNTDOWN CIRCUIT FOR CLEAN VERTICAL DEFLECTION
- INTEGRATED VERTICAL SAWTOOTH GENERATOR WITH AMPLITUDE CONTROL LOOP
- INTERLACE MODE CONTROLLED BY BUS
- VERTICAL SIZE CORRECTION (BREATHING) TO ADAPT DEFLECTION SENSITIVITY TO THE CURRENT BEAM (HIGH VOLTAGE VARIATION)
- BUS ADJUSTED VERTICAL PARAMETERS : VERTICAL AMPLITUDE, VERTICAL POSITION AND S-CORRECTION
- PANNING (SUBTITLE VERSION) FOR VERTICAL DEFLECTION



SHRINK 56
(Plastic Package)

ORDER CODE : STV2161

SCANNING PART (Continued)

- EAST-WEST FUNCTION GENERATOR WITH INTEGRATED ERROR AMPLIFIER (THUS, ONLY 1 EXTERNAL POWER DARLINGTON IS NECESSARY FOR EW FUNCTION)
- BUS CONTROLLED EAST-WEST FUNCTIONS : EW AMPLITUDE, HORIZONTAL WIDTH, EW TILT AND EW SHAPE (CORNER CORRECTION)
- VARIABLE FIX POINTS FOR S-CORRECTION VERTICAL BLANKING AND EAST-WEST CORNER CORRECTION
- SUPER SANDCASTLE OUTPUT (5V LEVEL) TO CONTROL OTHER CIRCUITS LIKE CHROMA DECODER, ...
- BUS REPLY FOR VIDEO IDENT, 50/60Hz VERTICAL MODE, TV STANDARD

SMPS PART

- SMPS PULSE WIDTH MODULATOR WITH BUS CONTROLLED REFERENCE VOLTAGE
- SOFT START FOR SMPS MODULATOR AND HORIZONTAL OUTPUT STAGE
- STANDBY OPERATION OF IC
- PROTECTION CIRCUIT FOR OVERLOAD DETECTION (SHORT-CIRCUITS) AND CONTROL OF SMPS MODULATOR
- BUS REPLY FOR OVERLOAD AND POWER FAIL

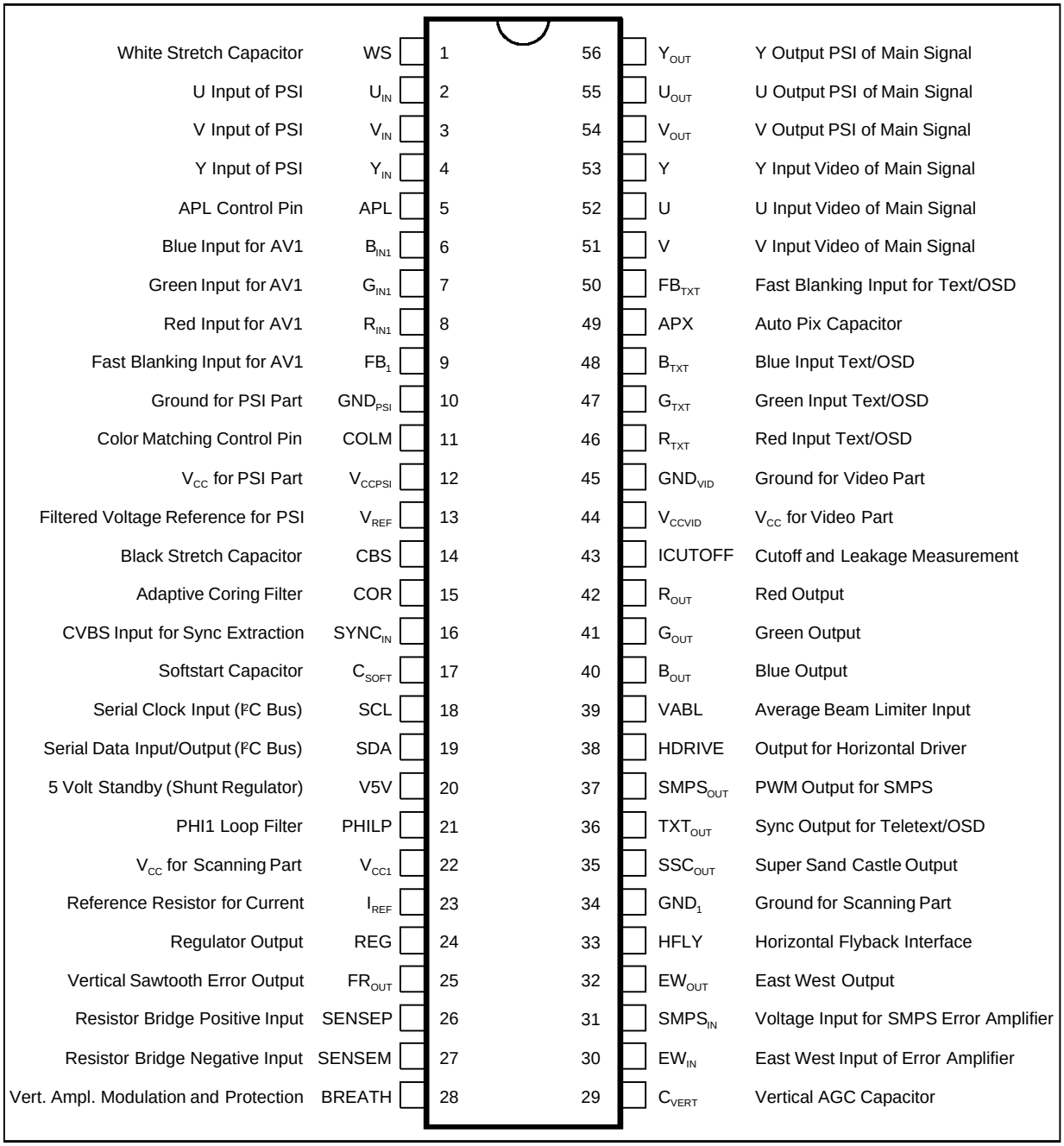
PSI PART

- EDGE REPLACEMENT FOR Y PATH
- PEAKING FOR Y PATH WITH ADAPTIVE CORING
- BLACK STRETCH FOR Y PATH WITH EXTERNAL TIME CONSTANT
- WHITE STRETCH FOR Y PATH WITH EXTERNAL TIME CONSTANT
- CTI (COLOR TRANSIENT IMPROVEMENT) FOR U AND V PATH
- COMPENSATION DELAY IN Y PATH FOR SIGNAL DELAY IN THE CHROMA PROCESSOR
- ALL FUNCTIONS CONTROLLABLE AND SWITCHABLE BY BUS

DESCRIPTION

The STV2161 is an I^2C bus controlled Video Scanning and PSI (Picture Signal Improvement) processor for 1H deflection (15.625kHz) television sets. The IC incorporates also an secondary SMPS (Switch Mode Power Supply) controller with soft-start and protection facilities.

PIN CONNECTION



2161-01.EPS

PIN DESCRIPTION

Pin N°	Symbol	Function	Description
1	WS	White Stretch Time Constant	External capacitor ; together with internal resistor of 200kΩ the time constant for White Stretch is realized.
2	U_{IN}	Input U Signal	DC value clamped via burst gate clamp. Input of PSI part.
3	V_{IN}	Input V Signal	DC value clamped via burst gate clamp. Input of PSI part.
4	Y_{IN}	Luma Input	Input pin for Luma ; DC value clamped via burst gate clamp. Input of PSI part.
5	APL	Control Pin for Auto Pedestal (APL)	External capacitor ; together with internal resistor of 200kΩ the time constant for auto pedestal is realized.
6	B_{IN1}	B1 Input	Video input blue (scart input).
7	G_{IN1}	G1 Input	Video input green (scart input)
8	R_{IN1}	R1 Input	Video input red (scart input).
9	FB_1	Fast Blanking Scart Input	Fast blanking input for SCART insertion : 0 = main picture, 1 = RGB SCART insertion if VS1, VS2 (BUS)= 0,1.
10	GND_{PSI}	Ground for PSI	Separated ground for PSI.
11	COLM	Control Pin for Color Matching	Pin has to be connected via resistor against ground. Resistor value determines color matching effect : 0 (short-circuit) = no effect, 30kΩ = maximal color matching.
12	V_{CCPSI}	V_{CC} for PSI	Separated V_{CC} for PSI.
13	V_{REF}	Voltage Reference	Pin should be connected via 100nF capacitor against ground (filtering of noise, stability, low impedance) reference voltage for PSI functions (Value = 3.85V).
14	CBS	Black Stretch Time Constant	External capacitor against ground forms together with the internal charging current the attack time of the black stretch detector. A resistor to V_{CC} realizes the decay time.
15	COR	Adaptive Coring Lowpass Filter	Internal resistor of 1kΩ builds with the external C the desired roll-off frequency (usually 500kHz to 3MHz).
16	$SYNC_{IN}$	Sync Separator Input	CVBS Input for sync separator, capacitor on the input serves as clamping capacitor for the black level.
17	C_{SOFT}	Softstart Capacitor	Capacitor for softstart, value determines softstart time.
18	SCL	Serial Clock for I^2C Bus	Data input (no pull down capability).
19	SDA	Serial Data for I^2C Bus	Data input and output (pull down capability for acknowledge and data reply).
20	V5V	Standby Biasing	Voltage supply for standby biasing of this IC, voltage is regulated via internal shun regulator.
21	PHILP	Horizontal Loop Filter	Loop filter for horizontal VCO (PHI1 loop filter).
22	V_{CC1}	Supply Voltage Scanning	Supply voltage for scanning part, connected with external series regulator transistor.
23	I_{REF}	Current Reference	External programming resistor 1% metal type (25kΩ against V_{CC1}) to determine the horizontal free running frequency.
24	REG	Control Pin for Regulator	Output for controlling the ext. series regulator transistor.
25	FR_{OUT}	Output for Frame Amplifier	Output of transconductance amplifier, pin has to be connected to the inverting input of the vertical power amplifier.
26	SENSEP	Sense Input, Positive	Input of internal resistor bridge for sensing the vertical deflection YOKE current.
27	SENSEM	Sense Input, Negative	Input of internal resistor bridge for sensing the vertical deflection YOKE current.
28	BREATH	Breathing Input	Multiple function : Input voltage = 1 to 7.7V = vertical size compensation. Pin pulled down by external transistor : protection activated. Test Mode : current between V_{CC1} and this pin (voltage drop <0.1V = sum of all DAC's).
29	C_{VERT}	Vertical AGC Capacitor	Regulation of vertical saw tooth amplitude.
30	EW_{IN}	EAST-WEST Input	Input of the error amplifier for the East-West modulator.
31	SMPSIN	SMPS Input	Input for the secondary switch mode power supply pulse width modulator.

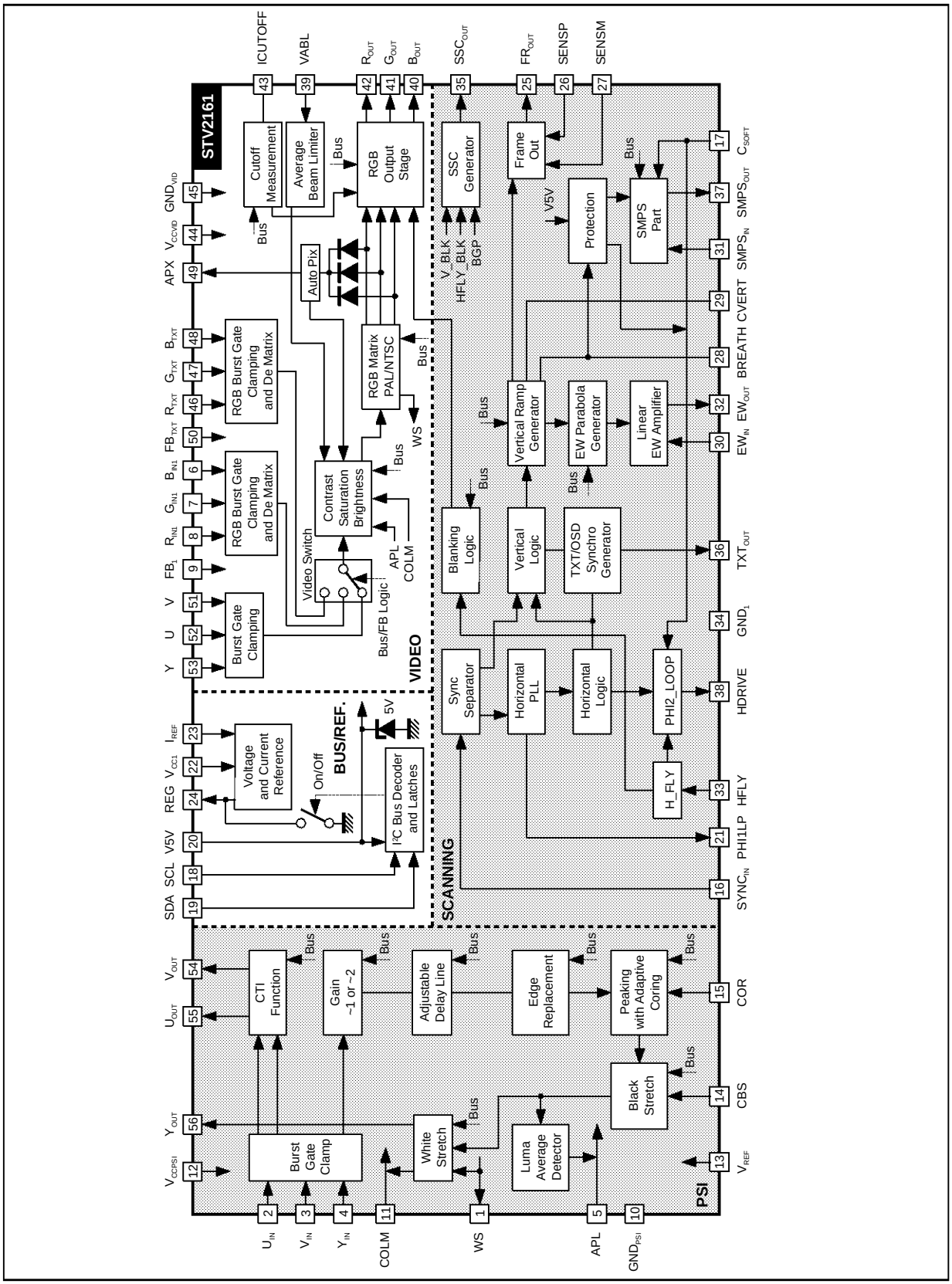
2161-01.TBL

PIN DESCRIPTION (Continued)

Pin N°	Symbol	Function	Description
32	EW_{OUT}	EAST-WEST Output	Output of the error amplifier for the East-West modulator (current output, biasing directly the darlington output transistor).
33	HFLY	Horizontal Flyback Input	Voltage input for horizontal flyback, polarity positive, one slicing level for Phi2 loop, blanking made with horizontal oversize blanking circuit.
34	GND_1	Ground Scanning	Ground for all scanning functions.
35	SSC_{OUT}	Super Sandcastle Output and Input	Super sandcastle output from the scanning processor part. It serves also as input for PSI and video part.
36	TXT_{OUT}	Multiple Logic Output	for MPX_2,1,0 = (000) this output is used as the TXT_Composite sync for TXT module and for OSD (µP). With the BUS register MPX_2,1,0, this output can deliver different logic signals (EWS and final test).
37	$SMPS_{OUT}$	SMPS Output	Output for SMPS driver transistor.
38	HDRIVE	Horizontal Output	Open collector output to drive the driver stage for the horizontal output transistor.
39	VABL	Average Beam Limiter	Voltage input for the average beam limiter function.
40	B_{OUT}	Blue Output	Video output blue channel.
41	G_{OUT}	Green Output	Video output green channel.
42	R_{OUT}	Red Output	Video output red channel.
43	I_{CUTOFF}	Cutoff Measurement Input	Input for the leakage and cutoff measurement. During the video time, the pin pulled up with ~0.5mA.
44	V_{CCVID}	Supply Voltage Video	Voltage supply for the video part.
45	GND_{VID}	Ground Video	Ground for video.
46	R_{TXT}	Red TXT Input	Input for red / channel of TEXT / OSD.
47	G_{TXT}	Green TXT Input	Input for green / channel of TEXT / OSD.
48	B_{TXT}	Blue TXT Input	Input for blue / channel of TEXT / OSD.
49	APX	Auto Pix Peak Detector	External capacitor and resistor to determine the attack and decay time of the APX detector.
50	FB_{TXT}	Fast Blanking TEXT Input	Fast-Blanking input for TXT/OSD - insertion (V_{FBTXT} = 0 to 3V). Threshold values of 5 and 7V for test mode.
51	V	V Input	Video input color difference signal V (B-Y).
52	U	U Input	Video input color difference signal U (B-Y).
53	Y	Y Input	Video input Y channel.
54	V_{OUT}	V Output Signal coming from PSI	Output impedance about 100Ω. Application : connect V_{OUT} with V (video part) via capacitor of 47nF.
55	U_{OUT}	U Output Signal coming from PSI	Output impedance about 100Ω. Application : connect U_{OUT} with U (video part) via capacitor of 47nF.
56	Y_{OUT}	Luma Output Signal	Output impedance about 100Ω. Application : connect Y_{OUT} with Y (video part) via capacitor of 47nF.

2161-01.TBL

BLOCK DIAGRAM



2161-02.EPS

I²C BUS CONTROL

I - Slave Address : hex 8C/8D

MSB							LSB
1	0	0	0	1	1	0	R/W

II - Write Mode

x = don't care bits, not used in the decoding of the subaddress.

Subaddress			Data Bits							
Binary	**Dec**	**Hex**	**MSB**							**LSB**
xxx00000	0	00			VID_ACT	S_ON	H_VCO			
xxx00001	1	01	PHI2_G0	PHI2_G1	S_VOLTAGE					
xxx00010	2	02	S_CORRECTION				EW_SHAPE			
xxx00011	3	03	0	0	EW_AMPLITUDE					
xxx00100	4	04	0	INTER_LACE	H_POSITION					
xxx00101	5	05	RES_FB	COMB_ON	EW_TILT					
xxx00110	6	06	AUTO_VCR	FORCE_VCR	H_WIDTH					
xxx00111	7	07	AY_1	AY_2	V_DC					
xxx01000	8	08	V_PAN	V_AMPLITUDE						
xxx01001	9	09	V_BLANKING				H_BLANKING			
xxx01010	10	0A	CT1_M1	CTI_M2	CTI_COR		CTI_GAIN			
xxx01011	11	0B	APL_LEVEL				ER_CORING			
xxx01100	12	0C	PK_CORI				PK_CORL			
xxx01101	13	0D	ER_M1	ER_M2	PEAKING					
xxx01110	14	0E	BS_OFF	WS_ON	WS_THRESHOLD					
xxx01111	15	0F	NTSC_PAL	BS_BL	CONTRAST					
xxx10000	16	10	VS1	VS2	BRIGHTNESS					
xxx10001	17	11	STOP_C_VAR	COLOR_OFF	SATURATION					
xxx10010	18	12	RGB_LIM		APX_THRESHOLD					
xxx10011	19	13	LUM_DEL1	Y_GAIN	R_CUTOFF					
xxx10100	20	14	LUM_DEL2	LUM_DEL3	G_CUTOFF					
xxx10101	21	15	RES_CUT	FUF	R_DRIVE					
xxx10110	22	16	HPOS_SEL	DIS_CUT	G_DRIVE					
xxx10111	23	17	0	0	B_DRIVE					

I^2C BUS CONTROL (Continued)

Subaddress 0 **hex 00**

Video Processor Activation / TV Mode Selection / Horizontal Freerunning Frequency

MSB							LSB
X	X	VID_ACT	S_ON	H3	H2	H1	H0

Switch to Activate Video Processor :

VID_ACT = 0 : Startup phase : video output (R, G, B_OUT) hard blanked (0.9V), no cutoff active

VID_ACT = 1 : RGB outputs active

Switch to Change from Standby Mode to Operation Mode :

S_ON = 0 : Standby operation : I^2C bus active ; protection logic active ; Pin REG pulled down to Ground

S_ON = 1 : TV-Set = ON : V_{CC} regulator active. This bus register can be forced by biasing the input FB_{TXT} with a voltage >5V (necessary for EWS test / final test)

Horizontal Freerunning Frequency :

H_VCO	0000 (hex 00)	Minimal free running frequency
	1111 (hex 0F)	Maximal free running frequency

Subaddress 1 **hex 01**

Phi2 Loop Gain Adjustment / System Voltage Adjustment

MSB							LSB
PHI2_G0	PHI2_G1	S5	S4	S3	S2	S1	S0

Gain of PHI2 Loop :

Relative Gain of PHI2 Loop	**PHI2_G1**	**PHI2_G0**
1 (Maximal)	0	0
0.666	0	1
0.4	1	0
0.25 (Minimal)	1	1

System Voltage Adjustment :

S_VOLTAGE	000000 (hex 00)	Minimal position : system voltage minimal
	111111 (hex 3F)	Maximal position : system voltage maximal

Subaddress 2 **hex 02**

"S" Correction / East-West Shape Correction

MSB							LSB
S3	S2	S1	S0	E3	E2	E1	E0

"S" Correction :

S_CORREC-TION	0000 (hex 00)	Minimal S-Correction (vertical sawtooth flat)
	1111 (hex 0F)	Maximal S-Correction

East-West Shape Correction :

EW_SHAPE	0000 (hex 00)	Minimal parabola flattening (ideal parabola)
	1111 (hex 0F)	Maximal parabola flattening (flattened corners of parabola)

Subaddress 3 **hex 03**

East-West Amplitude

MSB							LSB
0	0	E5	E4	E3	E2	E1	E0

East-West Amplitude :

EW_AMPLI-TUDE	000000 (hex 00)	Minimal parabola amplitude = 0V (= no parabola)
	111111 (hex 3F)	Maximal parabola amplitude = 0.7V

Subaddress 4 **hex 04**

Interlace Selection / Horizontal Picture Position

MSB							LSB
0	INTER_LACE	H5	H4	H3	H2	H1	H0

Interlace Mode :

INTER_LACE = 1 : Normal operation = interlaced ; incoming vertical sync pulses in interlace mode are maintained

INTER_LACE = 0 : Non-interlace operation ; incoming vertical sync pulses in interlace mode are shifted to the entire line position, thus interlaced signals are changed to non-interlaced vertical sync pulses

Horizontal Position :

H_POSITION	000000 (hex 00)	Minimal position : middle of HFLYBACK pulse +2.5µs before reference slope
	100000 (hex 20)	Nominal-position : middle of HFLYBACK pulse on reference slope
	111111 (hex 3F)	Maximal position : middle of HFLYBACK pulse -2.5µs after reference slope

I^2C BUS CONTROL (Continued)

Subaddress 5 hex 05

Fast Blanking 1 Detection Flipflops / Comb Filter Phi& Delay / East-West Unsymetry

MSB							LSB
RES_FB	COMB_ON	E5	E4	E3	E2	E1	E0

Reset Input of Fast Blanking Detection Flip-Flops :
RES_FB = 0 : Detection Flip-Flops sensibilized (ready to receive the information from FB_1 Pin)
RES_FB = 1 : Detection Flip-Flops reset to 0

Note : RES_FB can be read via reply bit : FBE_POS and FB_NEG.

Selection of Reference Slope for PHI1 Phase Comparator :
COMB_ON= 0 : PHI1 loop : rising edge of burst gate pulse = 2.8µs after middle of H-Sync
COMB_ON= 1 : PHI1 loop : rising edge of burst gate pulse = 4.15µs after middle of H-Sync

East-West Unsymetry :

EW_TILT	000000 (hex 00)	Minimal position : parabola unsymetrical (higher on the top of the picture)
	100000 (hex 20)	Parabola symetrical
	111111 (hex 3F)	Maximal position : parabola unsymetrical (lower on the top of the picture)

Subaddress 6 hex 06

TV/VCR Mode Selection / Horizontal Width

MSB							LSB
FORCE_ VCR	AUTO_ VCR	H5	H4	H3	H2	H1	H0

Line PLL Time Constante Choice :

FORCE _VCR	AUTO _VCR	TV Mode
0	0	PHI1 loop forced to NOVCR mode (TV operation)
0	1	VCR trick mode automatically detected and VCR mode forced (trick mode = not 312.5 lines per frame in 50Hz mode ; not 265.5 lines per frame in 60Hz mode)
1	0	Phi1 loop forced to VCR mode
1	1	Test mode for vertical countdown logic test (only EWS)

Picture Width :

H_WIDTH	000000 (hex 00)	Minimal position : DC_Value of parabola maximal
	111111 (hex 3F)	Maximal position : DC_Value of parabola minimal

Subaddress7 hex 07

Y Gain / Vertical Position

MSB							LSB
AY_1	AY_2	V5	V4	V3	V2	V1	V0

Luminance Gain :

Gain in Y Path	AY_1	AY_2
0dB	0	0
0.5dB	1	0
1dB	0	1
1.5dB	1	1

Vertical Position :

V_DC	000000 (hex 00)	Minimal position (picture shifted down by -0.065V on SENSP/SENSM)
	111111 (hex 3F)	Maximal position (picture shifted up by 0.065V on SENSP/SENSM)

Subaddress 8 hex 08

Vertical Panning / Vertical Sawtooth Amplitude

MSB							LSB
V_PAN	V6	V5	V4	V3	V2	V1	V0

Shift of Vertical Sawtooth 20 Lines Above for "SUB-TITLE" Application in ZOOM Mode :
V_PAN = 0 : no shift
V_PAN = 1 : Shift of 20 lines above

Vertical Amplitude :

V_AMPLI-TUDE	0000000 (hex 00)	Minimal amplitude ($0.46V_{PP}$ (between 190 lines) on SENSP/SENSM)
	1111111 (hex 7F)	Maximal amplitude ($1.16V_{PP}$ (between 190 lines) on SENSP/SENSM)

Subaddress 9 hex 09

Vertical Blanking / Horizontal Blanking

MSB							LSB
V3	V2	V1	V0	H3	H2	H1	H0

I²C BUS CONTROL (Continued)

Vertical Blanking :

V_BLANKING	0000 (hex 00)	Minimal value of fix points and vertical blanking (0.37V on SENSM/SENSP)
	1111 (hex 0F)	Maximal value of fix points and vertical blanking (0.6V on SENSM/SENSP)

Note : Changes vertical fix points for S-Correction and East-West parabola.

Horizontal Blanking :

H_BLANKING	0000 (hex 00)	Minimal horizontal oversize blanking (0µs)
	1111 (hex 0F)	Maximal horizontal oversize blanking (9µs on both sides)

Stepsize ~0.5µs ; first steps can be used to assure correct blanking in normal mode (since only 1 comparator (V_{CC}/4) on HFLY Pin is used).

Subaddress 10 hex 0A

Test Selection for CTI / CTI Coring / CTI Gain

MSB							LSB
CTI_M1	CTI_M2	COR1	COR0	CG3	CG2	CG1	CG0

CTI Function Enable :

CTI_M1	CTI_M2	Function	Signal on U_{OUT}/V_{OUT}
0	0	CTI off	Signal U or V passed through the delay line (380ns)
0	1	Reserved	
1	0	Reserved	
1	1	CTI on	CTI manipulated U, V signal

Slope of Transient Improvement Coring Level :

CTI_COR	00 (hex 0)	Minimal coring of CTI = ±25mV
	11 (hex 3)	Maximal coring of CTI = ±100mV

Slope of Transient Improvement Gain :

CTI_GAIN	0000 (hex 00)	Minimal gain of CTI (1) = slope flat
	1111 (hex 0F)	Maximal gain of CTI (6.5) = slope steep

Subaddress 11 hex 0B

Auto-Pedestal Level (Adaptive Brightness) / Edge Replacement Coring Value

MSB							LSB
A1	A2	A1	A0	E3	E2	E1	E0

Level of Adaptive Brightness :

APL_LEVEL	0000 (hex 00)	Minimal value = no influence = 0 IRE
	1111 (hex 0F)	Maximal value = maximal brightness increase (20 IRE for average value of 100 IRE)

Level of Edgereplacement Coring :

ER_CORING	0000 (hex 00)	Minimal coring level = highest sensibility
	1111 (hex 0F)	Maximal coring level = minimal sensitivity

Subaddress 12 hex 0C

Adaptive Coring for Peaking : Coring Intercept Point and Coring Level

MSB							LSB
I1	I2	I1	I0	L3	L2	L1	L0

Coring Intercept Point (Intercept Point where Coring for Peaking is Starting to Become Active) :

PK_CORI	0000 (hex 00)	Minimal intercept value
	1111 (hex 0F)	Maximal intercept value

Coring Level (Level of Coring for Peaking Function) :

PK_CORL	0000 (hex 00)	Minimal coring level = no coring
	1111 (hex 0F)	Maximal coring level = maximal coring

Subaddress 13 hex 0D

EDGE Replacement / Peaking Amplitude

MSB							LSB
ER_M1	ER_M2	P5	P4	P3	P2	P1	P0

Edge Replacement Enable :

ER_M1	ER_M2	Function	Signal on Output Y_{OUT} ; Passed Through Peaking Nad Black/White Stretch
0	0	Edge Replacement OFF	Signal Y passed through the delay line (70 + 90ns) ; no edge replacement
0	1	Reserved	
1	0	Reserved	
1	1	Edge Replacement ON	Edge replacement function active

I^2C BUS CONTROL (Continued)

PEAKING Amplitude :

PEAKING	000000 (hex 00)	Minimal peaking value (-6dB de-peaking)
	010101 (hex 15)	Frequency response flat (see Note)
	111111 (hex 3F)	Maximal peaking value (+6dB peaking)

Note : De-peaking path without coring ; peaking always with coring.
i.e. the middle position is not a neutral position :
de-peaking W/O corint & peaking w coring

Subaddress 14 hex 0E

Black Stretch ON/OFF / White Stretch ON/OFF / White Stretch Threshold

MSB							LSB
BS_OFF	WS_ON	W5	W4	W3	W2	W1	W0

Black Stretch Enable :
BS_OFF = 0 : Black stretch is active
BS_OFF = 1 : Black stretch is switched off

White Stretch Enable :
WS_ON = 0 : White stretch is switched off
WS_ON = 1 : White stretch is active

White Stretch Threshold :

WS_THRES-HOLD	000000 (hex 00)	Minimal position : threshold value = 5 IRE
	111111 (hex 3F)	Maximal position : threshold value = 40 IRE

Subaddress 15 hex 0F

RGB Matrix Selection / Black Level Choice for Black Stretch / Contrast

MSB							LSB
NTSC_PAL	BS_BL	C5	C4	C3	C2	C1	C0

Selection of RGB Matrix :
NTSC_PAL = 0 : RGB matrix uses the PAL/SECAM coefficients for the conversion YUV/RGB
NTSC_PAL = 1 : RGB matrix uses the NTSC coefficients for the conversion YUV/RGB

Note : The input de-matrix for RGB_{IN1} and RGB_{TXT} are always "PAL/SECAM" de-matrices.

Choice of Black Level Reference for Black Stretch :
BS_BL = 0 : BLACK = 0 IRE (PAL or SECAM mode)
BS_BL = 1 : BLACK = -7.5 IRE (NTSC mode)

Contrast Adjustment :

CONTRAST	000000 (hex 00)	Smaller contrast
	111111 (hex 3F)	Maximal contrast

Subaddress 16 hex 10

Priority Switch for RGB1 Insertion / Brightness

MSB							LSB
VS1	VS2	B5	B4	B3	B2	B1	B0

Priority Switch for RGB1 Insertion :

VS1	VS2	Priority Mode
0	0	Hard blanked RGB Outputs (= 0.9V) during video time, but cutoff measurement active!
0	1	Input = choice following the position of FB_1 (0 = YUV, 1 = RGB_{IN1})
1	0	Input = RGB_IN1
1	1	Input = YUV

Brigthness Adjustment :

BRIGHT-NESS	000000 (hex 00)	Minimal position : brightness = -30 IRE
	100000 (hex 20)	Nominal position : brightness = 0
	111111 (hex 3F)	Maximal position : brightness = +30 IRE

Subaddress 17 hex 11

Contrast Variation with TXT Insertion / Color Suppression / Saturation

MSB							LSB
STOP_C_VAR	COLOR_OFF	S5	S4	S3	S2	S1	S0

Relative TXT Contrast :
STOP_C_VAR = 0 : TXT/OSD insertion : same contrast as main channel
STOP_C_VAR = 1 : TXT/OSD insertion (FB2 = 1) toward max. CONTRAST and mid. SATURATION

Color Suppression :
COLOR_OFF = 0 : Picture with colors
COLOR_OFF = 1 : Picture without colors (U, V set to 0)

I^2C BUS CONTROL (Continued)

Color Saturation Adjustment :

SATURATION	000000 (hex 00)	Saturation is exactly 0 = minimal (<10%) but not completely suppressed colors
	111111 (hex 3F)	Maximal position : maximal saturation (3dB oversaturation)

Subaddress 18 hex 12

RGB Hard Limiter / Auto Pix (APX) Threshold Voltage

MSB							LSB
RGBLIM1	RGBLIM0	A5	A4	A3	A2	A1	A0

RGB Limiter (Voltage Limitation of R, G, B at the Output of the Matrix, just before DRIVE Adjustment) :

RGB_LIM	00 (hex 0)	Limitation at 100%
	11 (hex 3)	Limitation at 150%

Auto-Pix (APX) Threshold :

APX_THRESHOLD	000000 (hex 00)	Minimal position
	111111 (hex 3F)	Maximal position

Subaddress 19 hex 13

Luminance Compensation Delay / Luminance Gain / RED Cutoff Adjustment

MSB							LSB
LUM_DEL1	Y_GAIN	R5	R4	R3	R2	R1	R0

Compensation Delay of 45ns in the PSI Luma Path :

LUM_DEL1 = 1 : Delay of 45ns added additionally in the Luma path of PSI

LUM_DEL1 = 0 : No additional delay

Selection of Amplifier of Factor 2 in the Input of the Luma Path (PSI Part) :

Y_GAIN = 0 : Amplifier of factor 2 in the Luma path of PSI introduced (input voltage black white = $0.35V_{PP}$)

Y_GAIN = 1 : No amplifier in the Luma path of PSI (input voltage black white = $0.7V_{PP}$)

Cutoff Reference for Red :

R_CUTOFF	000000 (hex 00)	Insertion of 0.225V at R_{OUT} for red measurement pulse
	111111 (hex 3F)	Insertion of 0.675V at R_{OUT} for red measurement pulse

Note : Blue is fixed value of 0.45V at B_{OUT}.

Subaddress 20 hex 14

Luminance Compensation Delay / GREEN Cutoff Adjustment

MSB							LSB
LUM_DEL2	LUM_DEL3	G5	BG	G3	BG	BG	G0

Compensation Delay of 90ns in the PSI Luma Path :

LUM_DEL2 = 1 : Delay of 90ns added additionally in the Luma path of PSI

LUM_DEL2 = 0 : No additional delay

Compensation Delay of 180ns in the PSI Luma Path :

LUM_DEL3 = 1 : Delay of 180ns added additionally in the Luma path of PSI

LUM_DEL3 = 0 : No additional delay

Cutoff Reference for Green :

G_CUTOFF	000000 (hex 00)	Insertion of 0.225V at G_{OUT} for green measurement pulse
	111111 (hex 3F)	Insertion of 0.675V at G_{OUT} for green measurement pulse

Note : Blue is fixed value of 0.45V at B_{OUT}.

Subaddress 21 hex 15

Reset Cutoff / Cutoff Mode / RED Channel Gain (Drive)

MSB							LSB
RES_CUT	FUF	D5	D4	D3	D2	D1	D0

Reset of Cutoff Counters :

RES_CUT = 0 : Cutoff loop active

RES_CUT = 1 : Cutoff loop stopped and reset of all cutoff counters

Note : At the same time : stop of cutoff function.

Cutoff Loop Operation Mode :

FUF = 1 : Cutoff loop is active during the whole frame

FUF = 0 : Cutoff loop is active during the first 4 active video lines

RED Channel Gain (Drive) :

R_DRIVE	000000 (hex 00)	Minimal position : 0.33 of maximal value
	111111 (hex 3F)	Maximal position : $3.3V_{PP}$ at R_OUT for contrast = max and Y = $0.7V_{PP}$

I²C BUS CONTROL (Continued)

Subaddress 22 **hex 16**

Selection of Reference Slope for H_POSITION / Disable of Cutoff Loop / GREEN Channel Gain (Drive)

MSB							LSB
HPOS_SEL	DIS_CUT	D5	D4	D3	D2	D1	D0

Selection of the PHI2 Reference Slope :

HPOS_SEL = 1 : Reference slope = 2.7µs before rising edge of burst gate pulse

HPOS_SEL = 0 : Reference slope = rising edge of burst gate pulse

Activation of Cutoff-Loop :

DIS_CUT =0 : Cutoff loop is active

DIS_CUT =1 : Cutoff loop is stopped, actual values in the registers are frozen

Truth Table for DIS_CUT / FUF :

DIS_CUT	FUF	Operation Mode
0	0	Video signal present at RGB_{OUT} ; 3 cutoff measurement lines in the lines 21, 22, 23
0	1	Cutoff measurement during the whole frame with the sequence : leakage - red, green, blue (repetitive each 4th line)
1	0	Video signal present at RGB_{OUT} but no cutoff measurement (last values of cutoff conter frozen)
1	1	All outputs R_{OUT}, G_{OUT}, B_{OUT} hard blanked all the time ; no video ; no cutoff measurement (useful if TV is switched off : immediate stop of video output)

GREEN Channel Gain (Drive) :

G_DRIVE	000000 (hex 00)	Minimal position : 0.33 of maximal value
	111111 (hex 3F)	Maximal position : $3.3V_{PP}$ at G_OUT for contrast = max and Y = $0.7V_{PP}$

Subaddress 23 **hex 17**

Test Mode for PHI1 Mute Circuit / BLUE Channel Gain (Drive)

MSB							LSB
0	0	D5	D4	D3	D2	D1	D0

BLUE Channel Gain (Drive) :

B_DRIVE	000000 (hex 00)	Minimal position : 0.33 of maximal value
	111111 (hex 3F)	Maximal position : $3.3V_{PP}$ at B_OUT for contrast = max and Y = $0.7V_{PP}$

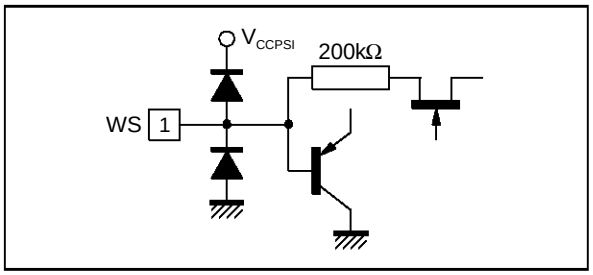
I^2C BUS CONTROL (Continued)

III - Read Mode

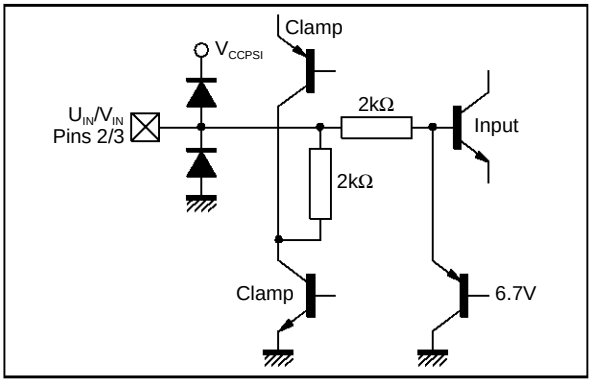
Reply Byte	MSB							LSB
1st	PON_RESET	OVER_LOAD	VID_ID	S60/50	V_STD	TUBE_COLD	FB_POS	FB_NEG
2nd	PHI1_MUTE	0	X	X	X	X	X	X
3rd	Not Def.	Not Def.	R_CUTOFF_COUNTER					
4th	Not Def.	Not Def.	G_CUTOFF_COUNTER					
5th	Not Def.	Not Def.	B_CUTOFF_COUNTER					

PON_RESET	1	If voltage drop on V5V (<4.5V) has been detected
OVERLOAD	1	If after 3 restart trials TV set is switched off definitely since breathing Pin was pulled down due to an error (reset to 0 can be done by switching off the TV set (S_ON = 0 ; see Subaddress 0)
VID_ID	1	If PHI1 PLL has locked
	0	If PHI1 PLL has not locked
S60/50	1	If vertical sync pulse frequency = 60Hz
	0	If vertical sync pulse frequency = 50Hz
V_STD	1	If line numbers per frame are interlace standard : exactely 312.5 (50Hz) or 262.5 (60Hz)
	0	If line numbers per frame are different from this standard VCR trick mode recognition
TUBE_COLD	1	After start of TV set
	0	If the first time one of the cutoff counters is decremented (tube starts to deliver beam current)
FB_POS	1	If fast blanking FB_1 was set to 1 ; reset can be done by activating the bit RES_FB (see Subaddress 5)
FB_NEG	1	If fast blanking FB_1 was set to 0 ; reset can be done by activating the bit RES_FB (see Subaddress 5)
PHI1_MUTE	1	If HVCO is in the MUTE mode (no valid sync detected) ; PHI1LP connected to $V_{CC}/2$
	0	If PLL of HVCO is in CAPTURE or LOCK mode
R_CUTOFF_COUNTER		Returns the 6 MSB bits of the red cutoff counter
G_CUTOFF_COUNTER		Returns the 6 MSB bits of the green cutoff counter
B_CUTOFF_COUNTER		Returns the 6 MSB bits of the blue cutoff counter

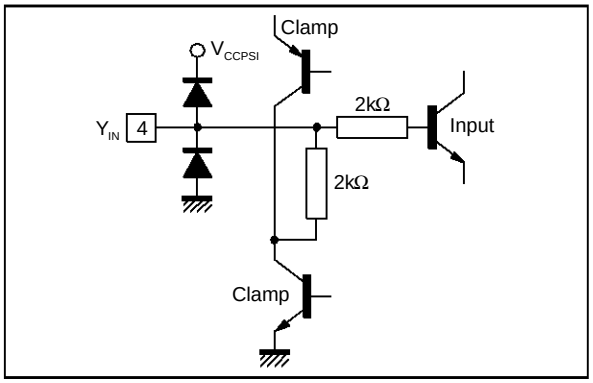
INTERNAL SCHEMATICS



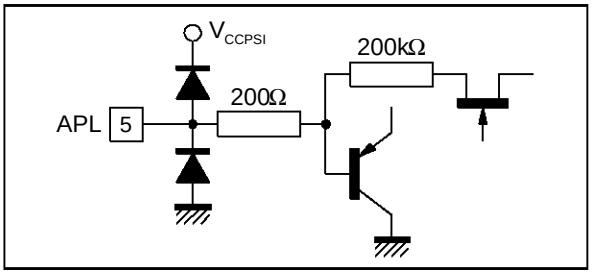
2161-03.EPS



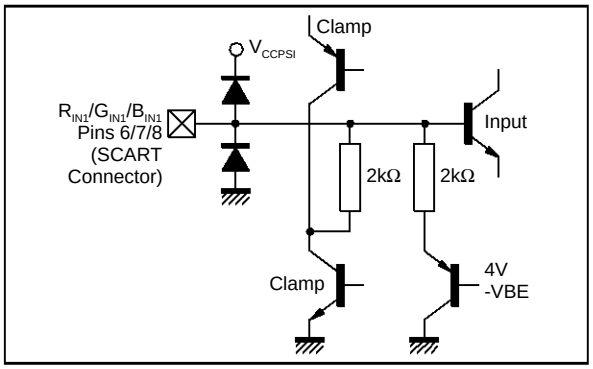
2161-04.EPS



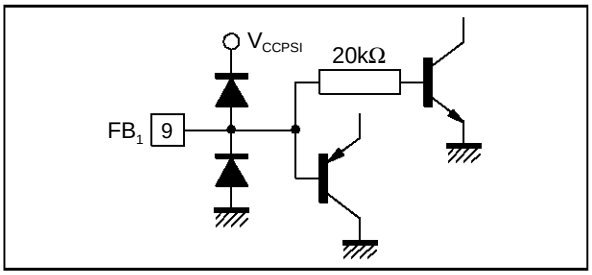
2161-05.EPS



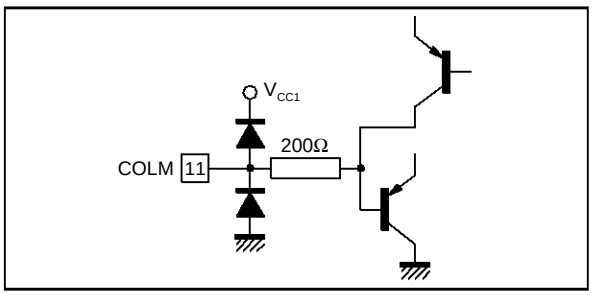
2161-06.EPS



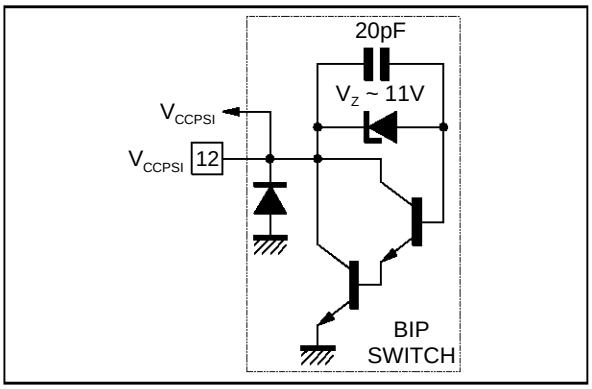
2161-07.EPS



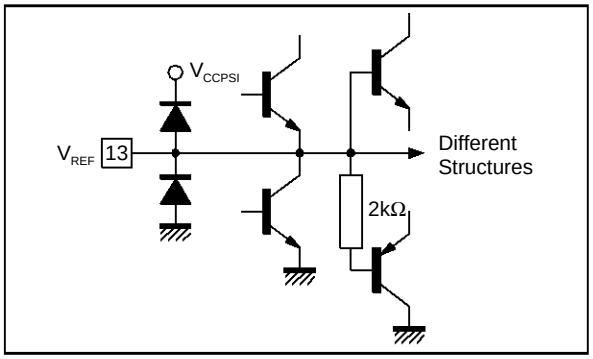
2161-08.EPS



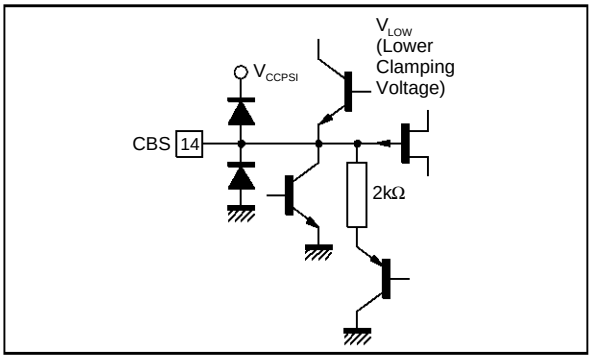
2161-09.EPS



2161-10.EPS

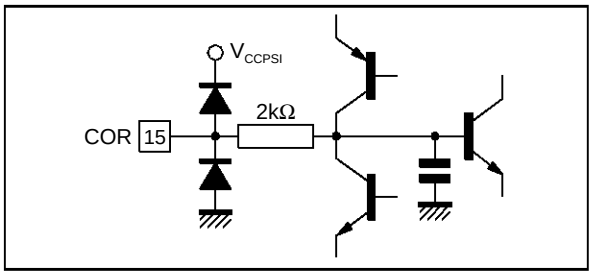


2161-11.EPS

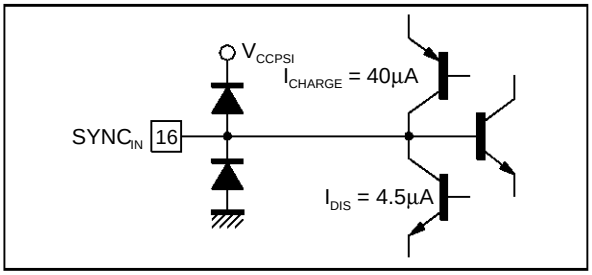


2161-12.EPS

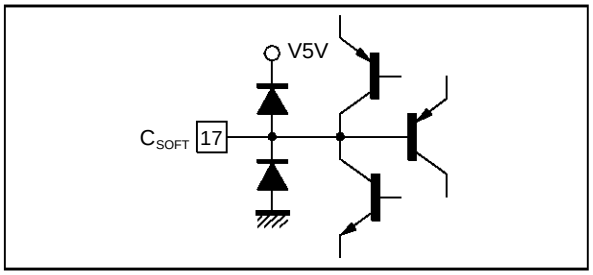
INTERNAL SCHEMATICS (Continued)



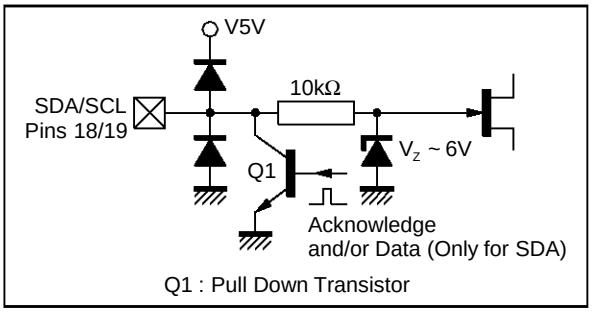
2161-13.EPS



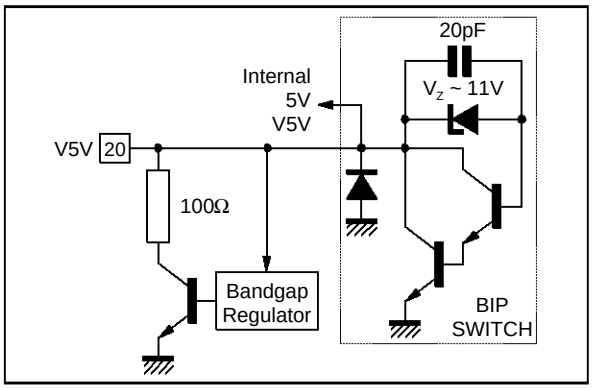
2161-14.EPS



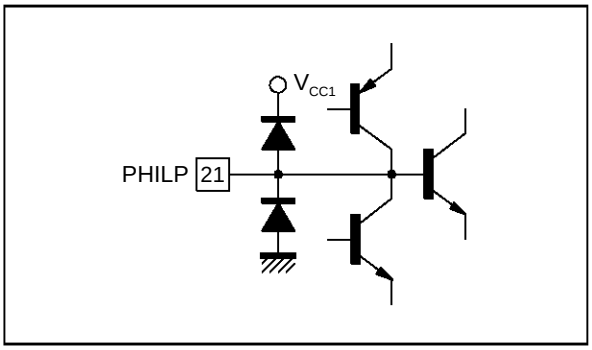
2161-15.EPS



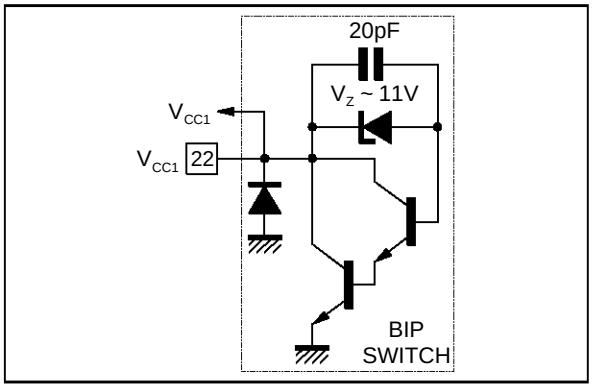
2161-16.EPS



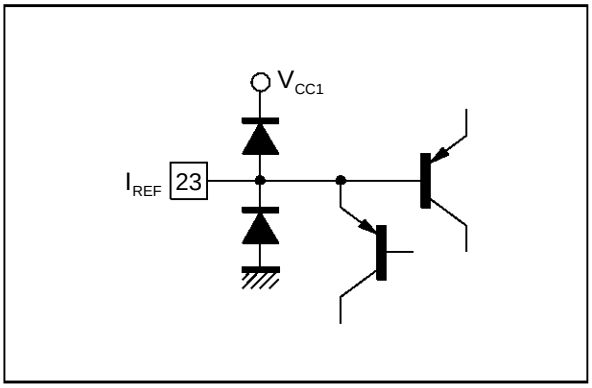
2161-17.EPS



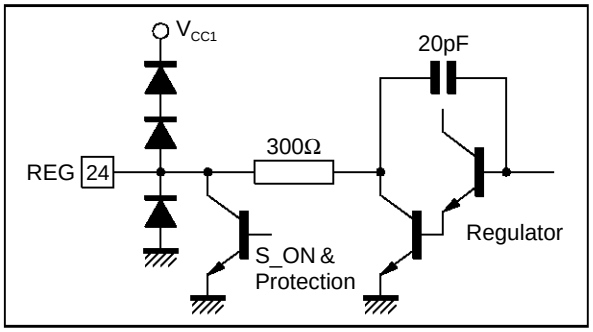
2161-18.EPS



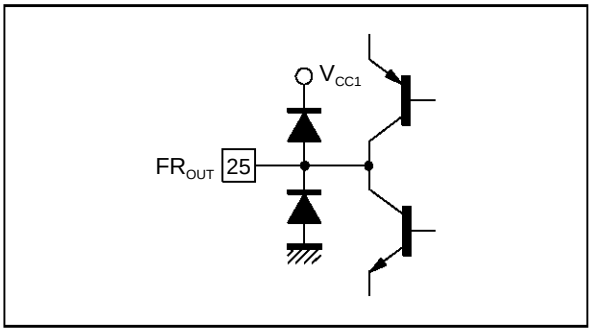
2161-19.EPS



2161-20.EPS

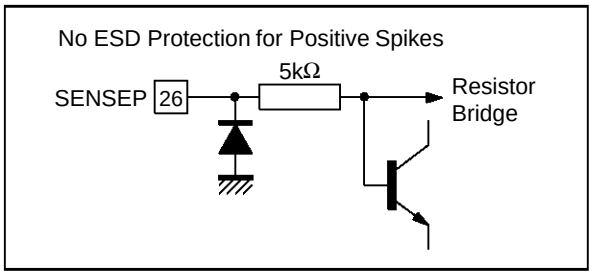


2161-21.EPS

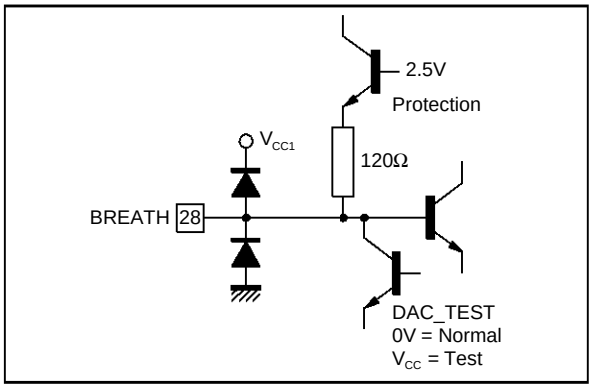


2161-22.EPS

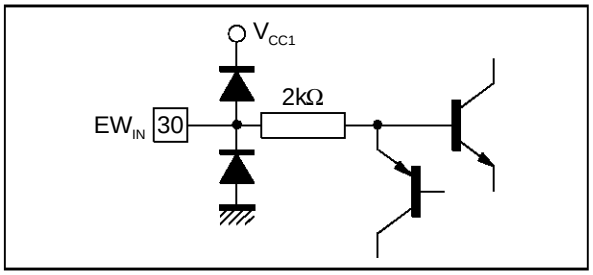
INTERNAL SCHEMATICS (Continued)



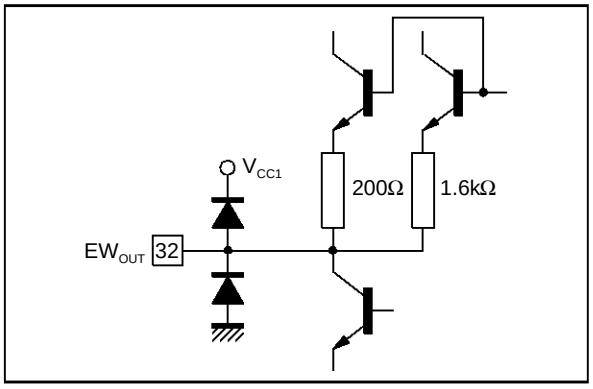
2161-23.EPS



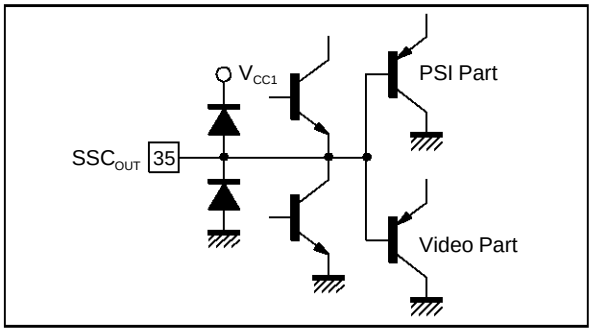
2161-25.EPS



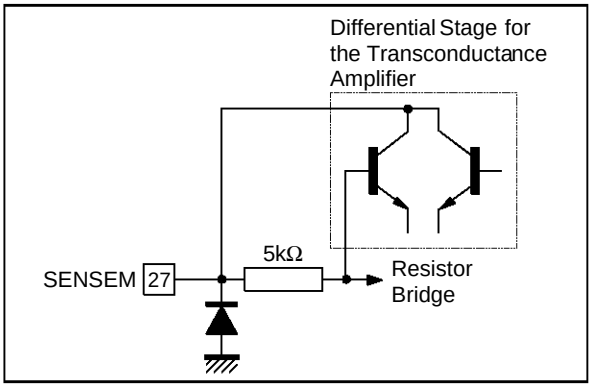
2161-27.EPS



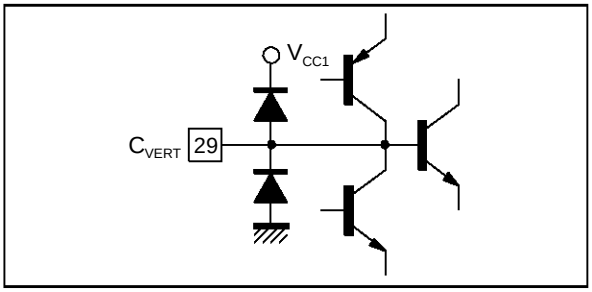
2161-29.EPS



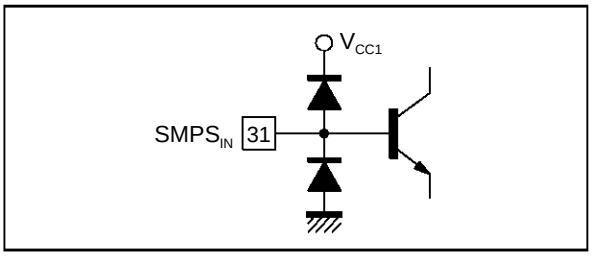
2161-31.EPS



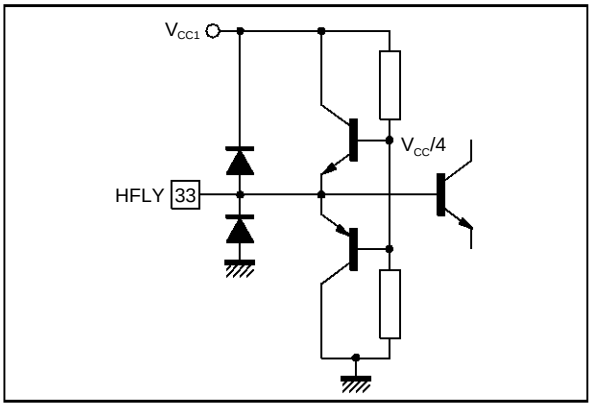
2161-24.EPS



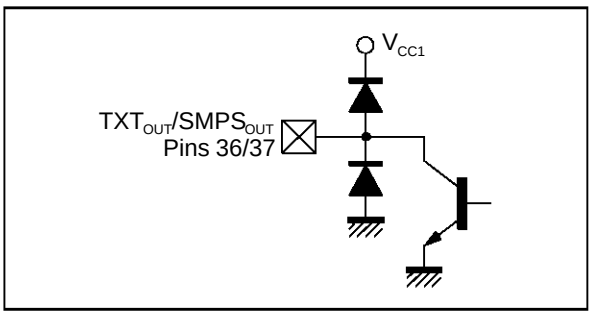
2161-26.EPS



2161-28.EPS

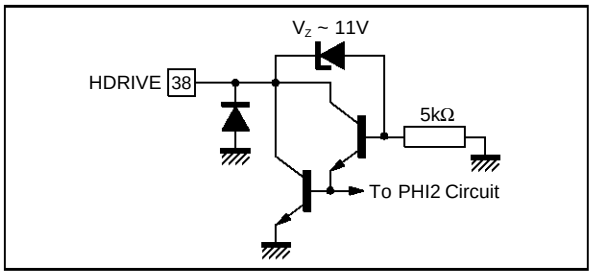


2161-30.EPS

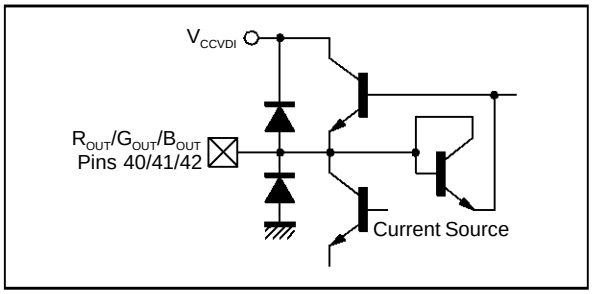


2161-32.EPS

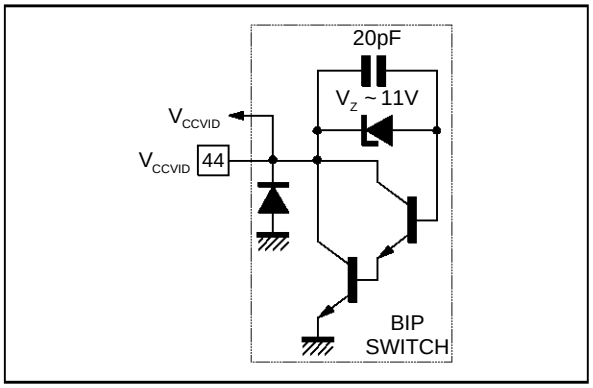
INTERNAL SCHEMATICS (Continued)



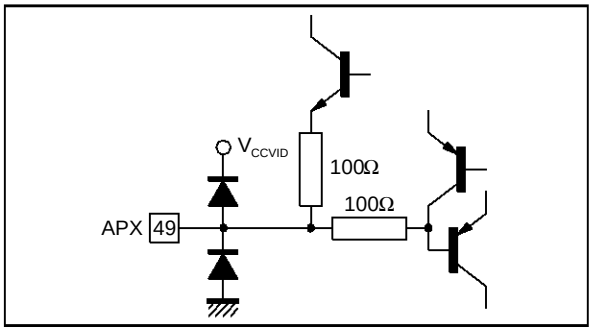
2161-33.EPS



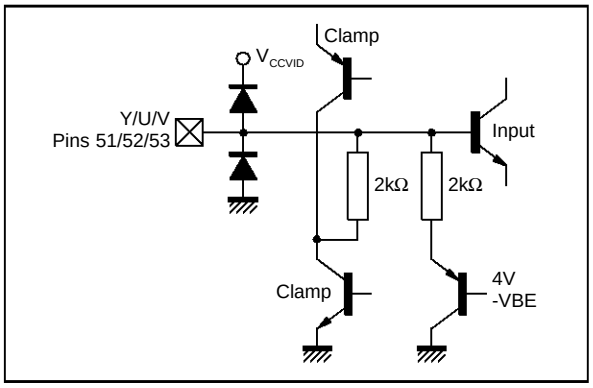
2161-35.EPS



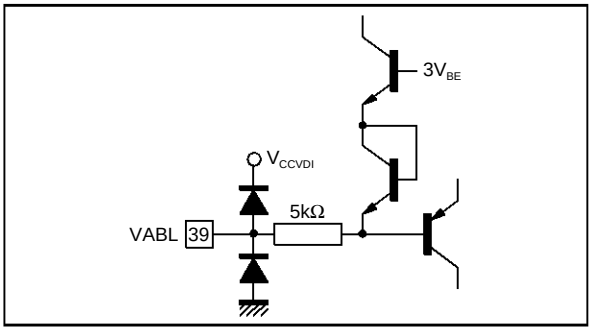
2161-37.EPS



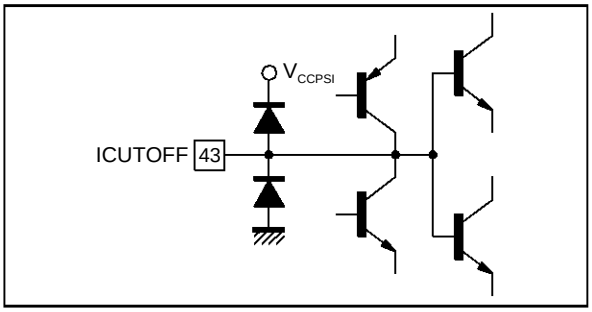
2161-39.EPS



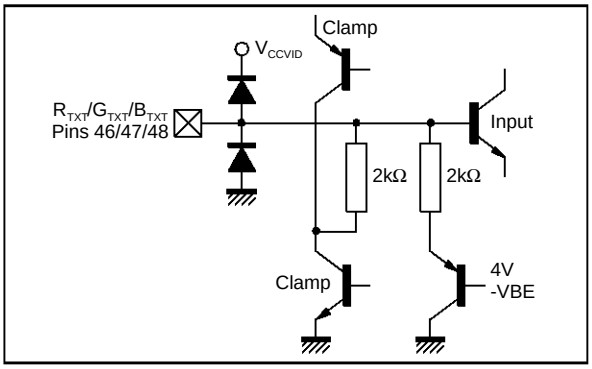
2161-41.EPS



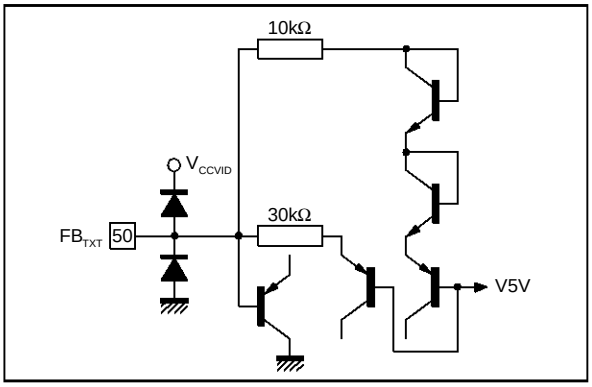
2161-34.EPS



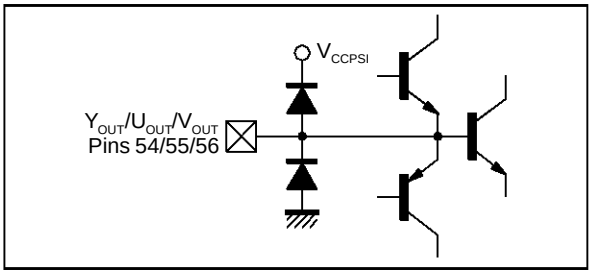
2161-36.EPS



2161-38.EPS



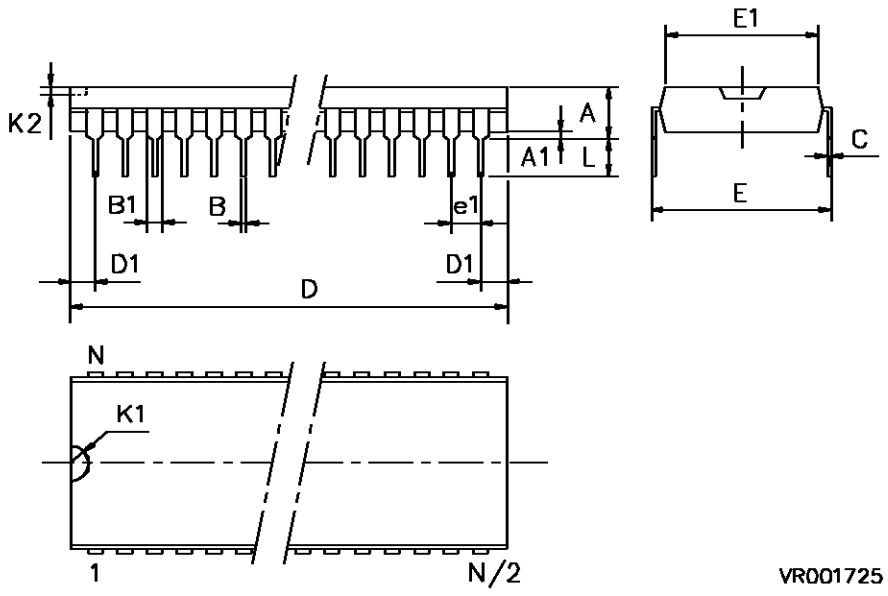
2161-40.EPS



2161-42.EPS

PACKAGE MECHANICAL DATA

56 PINS - PLASTIC SHRINK DIP



PMSDIP56.EPS

Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			5.08			0.200
A1	0.51			0.020		
B	0.35		0.59	0.014		0.023
B1	0.75		1.42	0.030		0.056
C	0.20		0.36	0.008		0.014
D		52.12			2.052	
D1	–	–	–	–	–	–
E			18.54			0.730
E1		13.72				0.540
K1	–	–	–	–	–	–
K2	–	–	–	–	–	–
L	2.54		3.81	0.100		0.150
e1		1.78			0.070	

SDIP56.TBL